System and Method for Sharing Memory by Heterogeneous Processors

ABSTRACT

A system for sharing memory by heterogeneous processors, each of which is adapted to process its own instruction set, is presented. A common bus is used to couple the common memory to the various processors. In one embodiment, a cache for more than one of the processors is stored in the shared memory. In another embodiment, some of the processors include a local memory area that is mapped to the shared memory pool. In yet another embodiment, local memory included on one or more of the processors is partially shared so that some of the local memory is mapped to the shared memory area, while remaining memory in the local memory is private to the particular processor.